Q27-Trilith: Compilation and Post-Layout Evaluation of SKY130A Ternary Circuits and Track-B pack5 Datapaths

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Abstract—Balanced ternary logic ($T = -1, 0, +1$; $V_{SS} = 0\,\mathrm{V}$, $V_{MID} = V_{DD}/2$, V_{DD}) offers 36.9% asymptotic interconnect reduction and multiplier-free 1.58-bit inference, yet layout-extracted open-PDK validation remains scarce. We present Q27-Trilith (v3.2.28), a typed hardware compiler and evaluation suite spanning ten experiment families (EXP-01..EXP-10). All native SKY130A layouts were evaluated by open-PDK extraction and BSIM4.5 simulation (Track B by Yosys/OpenSTA); no fabricated Q27 die was measured. A sub-rail 29T standard ternary inverter (q27_STI_HF) reduces nominal matched post-layout state-0 static power $\approx 1{,}000\times$ ($14.573\,\mu\mathrm{W} \to 14.57\,\mathrm{nW}$, both supplies), passes 75/75 extracted PVT DC-window corners (NM $\geq 15.43\%\,V_{DD}$), and lowers linearly interpolated 15 fF $1 \to T$ mid-band crossing time to 69.7 ps. Across 25 DRC-clean, LVS-matched SKY130A cell types (9 baseline, 16 Q27-compiled; 2T–100T), we evaluate SC 2:1 V_{MID} delivery, 0-shielded buses, decoupled T-SRAMs, Kleene guards, a 68T multiplier, a 100T half-adder, and an externally supported 707T two-term dot-product core (250.15/244.52 nW TT standby). On binary-hosted Track B, Q27-compiled pack5 (1.60 b/w) cuts 10-weight MAC synthesis area by 58.3% and xc7 LUTs by 57.5% vs. INT4; a routed pipeline met 12 ns 9-corner OpenSTA setup/hold and electrical checks (0/0/0 slew/cap/fanout; 107.5/214.8 MHz SS/TT) plus physical DRC, LVS, and antenna checks.

Index Terms—Balanced ternary logic, SKY130A, post-layout RC PEX, sub-rail ternary inverter, switched-capacitor mid-rail regulator, ternary SRAM, single-event upset, Kleene logic, hardware compiler, BitNet b1.58, pack5 accelerator.

I. Introduction

INTEREST in radix-3 hardware has grown alongside 1.58-bit balanced ternary neural networks (BitNet b1.58 [1], TerEffic [2], TABv2 [3]) and ternary post-quantum cryptography (SCOPE [4]). Recent studies span band-to-band tunneling (BTBT) T-CMOS [5]–[7], threshold-switch P-TMOS [8], multi-V_{th} CNTFET and CMOS MVL arithmetic [9]–[11], and fabricated 40-nm charge-domain [12] and 28-nm ternary-latch CIM silicon [13]. However, native circuit studies rarely combine open-PDK post-layout RC parasitic extraction (PEX), skewed-corner checks, mid-rail power delivery, and automated layout compilation, while binary-hosted accelerators [2], [14] do not explore multi-level physical trade-offs.

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Throughout this work, balanced ternary digits $\{T, 0, +1\}$ denote $\{-1, 0, +1\}$ mapped to $\{V_{SS} = 0\,\mathrm{V}, V_{MID} = V_{DD}/2, V_{DD}\}$. Q27-Trilith [15] (v3.2.28) pairs a single-source-of-truth (SSOT) hardware compiler with two complementary paths evaluated in open-source tools (ngspice-47, SkyWater SKY130A [16], KLayout 0.30.7, Magic 8.3, Netgen 1.5, Yosys 0.62, OpenROAD, and LibreLane 3.0): Track A / A+ (native 3-level SKY130A layouts plus compact-model projections to 22-nm FD-SOI and 28-nm BTBT) and Track B (binary-hosted pack5 1.60-bit/trit datapaths). Our contributions span ten experiment families (EXP-01..EXP-10):

1) SPICE Power Forensics & Sub-Rail q27_STI_HF (EXP-01..03, 05B/C, 06A): Identifies point-to-point method=trap numerical ringing and implements 29T planar q27_STI_HF and 28T triple-well q27_STI_HF_TW, reducing nominal matched both-supply PEX state-0 static power $\approx 1{,}000\times$ ($14.573\,\mu\mathrm{W} \to 14.57\,\mathrm{nW}$), passing 75/75 extracted PVT DC-window corners, and cutting 15 fF $1 \to T$ mid-band crossing duration (0.65–1.15 V) 10.77× to 69.7 ps.
2) V_{MID} Power Delivery & 0-Shielded Buses (EXP-04, 06B): Benchmarks an interleaved SC 2:1 divider across five corners (≤ 24.13 mV on 32/32 and 48/16 bursts; 44.62 mV on 64/0) and lumped 0-shielded 1.5 mm met2 coupling (≤ 52.06 mV victim excursion).
3) 25 Extracted SKY130A Cell Types (EXP-05, 05B–05L): Verifies 25 distinct DRC-clean, LVS-matched layouts (9 Python-constructed baseline cells and 16 Q27 v3.2.28-compiled cells, 2T–100T), including q27_TSRAM_60T_Z3 (EXP-05I/J), q27_KLEENE_GUARD_HF (EXP-05H), 68T q27_TMUL_Z3 (EXP-05K), 100T balanced half-adder q27_THA_Z3 (EXP-05L), and 7 StrongARM periphery cells (EXP-05G).
4) Memory Retention, Fault Injection, & Core Integration (EXP-07, 05D–05G, 09C–09G): Restores modeled Read-SNM_0 via 2T decoupled ports, quantifies state-0 single-event upset (SEU) Q_{crit} asymmetry and 60T/42T Kleene guard containment, and integrates progressively larger externally supported native blocks (09C/D 215T, 09E 471T 4-cell bank, 09F 607T two product lanes, and 09G 707T two-

term dot-product core).

5) Q27 v3.2.28 Compiler, TDD+TMG, & Track-B pack5 (EXP-08..10): Implements 9 compile-time checks (17 seeded errors detected), Ternary Decision Diagram (TDD) sifting with Ternary Multi-valued Gate (TMG) mapping, SAT-checked pack5 fault clamping, Yosys 0.62 ASIC/FPGA synthesis, LibreLane 3.0 P&R (0/0/0 slew/cap/fanout across 9 OpenSTA corners plus 0 physical DRC/LVS/antenna violations), and a matched-energy analytical cross-technology PPA model.

II. SPICE Forensics and Sub-Rail q27_STI_HF

A. EXP-01: Resolving the Transient Power Discrepancy

Prior SKY130A ternary testbenches reported large differences between DC (0.38 μW) and instantaneous transient (28.8 μW) state-0 power. Sweeping ngspice-47 integration settings shows that default trapezoidal integration (method=trap) induces $\pm 58.0\,\mu$W (q27_STI) and $\pm 65.8\,\mu$W (an external 33T tern_sti schematic reference) point-to-point numerical ringing on $i(V_{DD})$ (although time-averaged trapezoidal power converges toward DC). Switching to option method=gear reltol=1e-4 suppresses sample ringing to $< 0.001\%$ relative to DC .op, yielding schematic state-0 power of 14.880 μW (q27_STI, V_{DD} rail) and 0.382 μW (33T reference). On $T \to 0$ ($C_L = 100\,$fF), static-subtracted net energy across ideal supplies is $-80.45\,$fJ, reflecting charge return into the ideal V_{MID} source.

B. EXP-02 & EXP-03/06A: Sub-Rail Zero-Crowbar q27_STI_HF

Across 75 SKY130A PVT corners ($\{$tt,ff,ss,fs,sf$\} \times \{-40, -20, 27, 85, 125\}^\circ$C$\times\{1.62, 1.80, 1.98\}$ V), nine baseline cells passed 4,725/4,725 functional checks ($|\Delta V(0)| \leq 9.51\,$mV, observed max 9.508 mV), while the baseline 20T q27_STI passed 70/75 corners at $\min \text{NM} \geq 10\%\,V_{DD}$ and 55/75 at $\geq 15\%\,V_{DD}$, dropping to $\text{NM}_0 = 100\,$mV ($6.17\%\,V_{DD}$) at sf/-40°C/1.62 V. Separately, an empirical behavioral 1.8 V/50 nA BTBT deck (15 mV threshold spread, 1,000 samples per $\sigma_{I_{BTBT}}$ setting across 10 settings; distinct from Table V's 1.0 V/18 nA analytical profile) yields $\sigma_{I_{BTBT}} \leq 1.5\%$ for $\pm 5\%\,V_{DD}$ centering ($\leq 5.0\%$ for NM $\geq 180\,$mV).

To address state-0 crowbar current, skewed-corner collapse, and mid-band crossing duration simultaneously, we designed q27_STI_HF (29 logical MOSFETs, 35 extracted fingers; Fig. 1a) in stdlib/tscl_silicon.q27: (i) split input detectors operate strictly on sub-rails $[V_{SS}, V_{MID}]$ (isolated nwell=V_{MID}) and $[V_{MID}, V_{DD}]$ with feed-forward level shifters (avoiding cross-coupled latches that hinder DC convergence), cutting off both rail paths at $V_{in} = V_{MID}$; (ii) a parallel LVT PMOS helper ($M_{p,ph1l} = 0.42/1.35\,\mu$m) prevents cold-corner SVT cutoff while $2.5\times$ C_{dh} scaling cuts schematic cold delay $1.71\times$ ($20.6 \to 12.0\,$ns); (iii) a joint $\text{NOR}_2(l, h)$ and asymmetric inertial rise filter enable the V_{MID} transmission gate while suppressing transient V_{MID} turn-on during $T \leftrightarrow 1$ transitions (while l_b and h directly drive pull-up $M_{p,pu}$ and pull-down $M_{n,pd}$, Fig. 1a). In Fig. 1b–d, q27_STI_HF passes 75/75 schematic PVT DC-window corners ($\min \text{NM} = 260\,\text{mV} = 16.05\%\,V_{DD}$), 1,000/1,000 schematic tt_mm mismatch samples ($\min \text{NM} \geq 400.0\,$mV), and consumes 14.55 nW schematic ($1{,}022\times$ below matched 14.876 μW) and 14.57 nW nominal tt PEX ($1{,}000\times$ below matched 14.573 μW), both counting V_{DD} and V_{MID} supplies. At $C_L = 15\,$fF, linearly interpolated time spent in the 0.65–1.15 V mid-band during $1 \to T$ (2 ps max step, matched estimator on both extracted cells) is 40.8 ps schematic and 69.7 ps PEX ($10.77\times$ below 750.4 ps baseline PEX; an earlier 20 fF schematic sweep gave 36.4 ps).

III. Mid-Rail V_{MID} Delivery and 0-Shielded Buses

A. EXP-04: Interleaved Switched-Capacitor 2:1 vs. Class-AB

Driving 64 q27_STI cells (1,280 BSIM4.5 MOSFETs) without an ideal V_{MID} source across 5 process corners (1.8 V, 27°C, initialized storage, ideal 100 MHz clocks and capacitors, Fig. 2), an interleaved 2-phase SC 2:1 divider ($C_{fly} = 2 \times 4\,$pF, $C_{tank} = 20\,$pF) holds peak absolute mid-rail error to 4.16–24.13 mV ($\leq 1.34\%\,V_{DD}$, meeting our 35 mV design target) for balanced 32/32 and asymmetric 48/16 bursts, with a signed regulator-to-array supply-power ratio of -1.16% to $+2.74\%$ ($\approx 7.5\times$ lower than Class-AB in balanced tt; Class-AB shows 4.6–16.4% ratio, $A_{DC} = 73.0\,$dB, and PM = 50.35°, short of our 60° target). Under an extreme unipolar 64/0 burst, however, SC 2:1 error exceeds the 35 mV design target at all 5 corners (reaching 44.62 mV at fs), bounding unsupported burst asymmetry.

B. EXP-06B: Lumped 1.5 mm met2 Crosstalk & 0-Shielding

On a lumped 1.5 mm SKY130A met2 line model ($R = 600\,\Omega$, $C_g = 120\,$fF) with simultaneous $T \leftrightarrow 1$ dual aggressors (Fig. 3), unshielded coupling at $C_c/C_g = 0.45$ produces a 740.31 mV victim excursion and 949.58 mV baseline receiver upset, whereas q27_STI_HF limits receiver response to 0.26 mV. At $C_c/C_g = 0.65$ (899.45 mV victim excursion), both receivers upset (952.22 mV baseline; 1,014.07 mV q27_STI_HF). Modeling V_{MID} 0-shielding via reduced coupling cuts peak victim excursion $17.28\times$ to 52.06 mV, with 0.05 mV (baseline) and 0.00 mV (q27_STI_HF) modeled receiver responses.

IV. Post-Layout RC PEX and Ring Oscillator Dynamics

Twenty-five distinct SKY130A cell types (2T–100T, Table I)—comprising 9 Python-constructed baseline layouts (EXP-05) and 16 Q27 v3.2.28-compiled layouts (EXP-05B–05L)—were verified with 0 DRC violations (sky130A_mr.drc), unique LVS match (24 KLayout + 1 Magic 8.3/Netgen 1.5 triple-well), and Magic 8.3 RC extraction (cthresh 0, extresist on). Alongside the 9 baseline cells, planar 29T q27_STI_HF, triple-well 28T

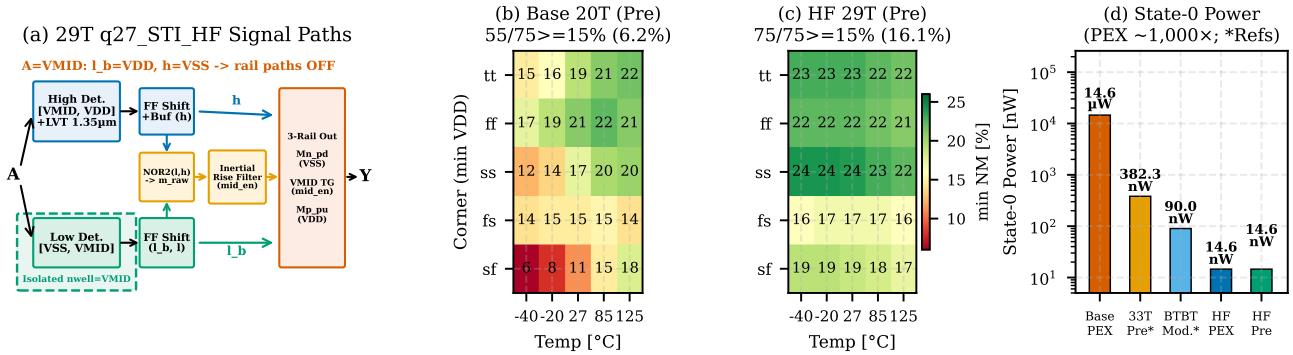

Fig. 1. EXP-03/05B/06A SKY130A inverter evaluation: (a) True 3-branch signal architecture of 29T q27_STI_HF showing isolated nwell=V_{MID} low-detector ($l_b \to M_{p,pu}$), high-detector with LVT helper ($h \to M_{n,pd}$), and joint $\mathrm{NOR}_2(l,h)$ feeding the inertial rise filter into the V_{MID} transmission gate; (b) Schematic 20T q27_STI DC window (55/75 $\geq$ 15%, 70/75 $\geq$ 10%, worst 6.2% at sf); (c) Schematic 29T q27_STI_HF (75/75 $\geq$ 16.05% pre, $\geq$ 15.43% PEX; 1,000/1,000 pre tt_mm MC); (d) State-0 static power showing matched SKY130A PEX ($\approx$ 1,000×, 14.573 μW $\to$ 14.57 nW) alongside auxiliary 33T schematic and BTBT model references (*).

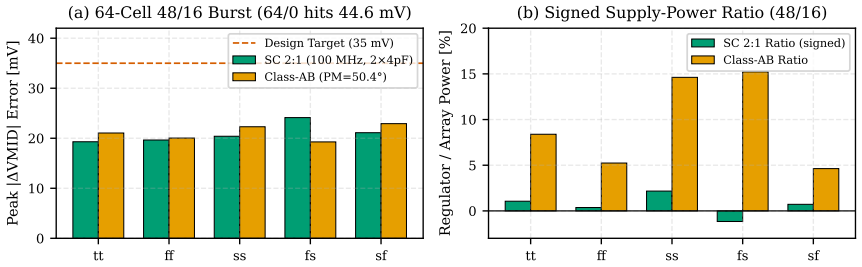

Fig. 2. EXP-04 on-chip V_{MID} regulation driving 64 SKY130A q27_STI cells (1.8 V, 27°C, ideal clocks/capacitors): (a) 48/16 burst peak $|\Delta V_{MID}|$ vs. 35 mV design target (64/0 hits 44.62 mV); (b) signed regulator-to-array supply-power ratio.

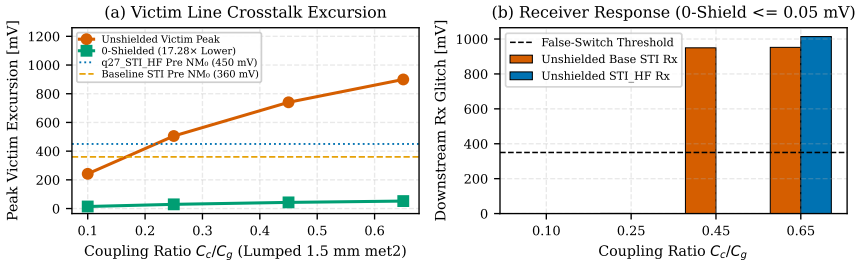

Fig. 3. EXP-06B lumped 1.5 mm SKY130A met2 crosstalk bench: (a) unshielded vs. 0-shielded victim excursion ($\leq$ 52.06 mV); (b) downstream receiver glitch response (0.05/0.00 mV when 0-shielded).

q27_STI_HF_TW, 46T/56T/60T T-SRAMs, 60T/42T Kleene guards, and 7 periphery macros, two Q27-compiled zero-crowbar arithmetic blocks complete the compute suite: 68T q27_TMUL_Z3 (EXP-05K, 2,582.1 μm^2, 9 input pairs × 5 corners = 45/45 pass, 12.78 nW TT average weighted by assumed $p_0 = 0.55$ vs. 16.04 μW in a 40T STI+TMUX implementation [1,255× TT ratio], TT worst-input 14.88 nW, ss/125°C max 249.4 nW) and 100T balanced ternary half-adder q27_THA_Z3 (EXP-05L, 3,190.0 μm^2, 45/45 dual-output checks, 15.02 nW TT weighted avg, TT worst-input 16.89 nW, ss/125°C max 184.21 nW, selected carry/sum arcs 0.923/1.126 ns).

In ngspice-47 (C_L = 15 fF, Fig. 4), 20T q27_STI exhibits 2.01–2.86× PEX delay scaling and 2.12× longer $1 \to T$ mid-band crossing (354.4 $\to$ 750.4 ps, linearly interpolated at 2 ps max step). In EXP-05B, planar 29T q27_STI_HF (202 R/189 C, 172.0 fF, 35 fingers) corrected a +15 mV multi-finger bin shift on $V_{th,lo}$ via $M_{n,nl1}/M_{p,pl1}$ co-sizing, passing 75/75 PEX DC-window corners ($\geq$ 15.43% V_{DD}, verifying full rail-to-rail sweeps, all four crossings, and rail endpoints within 2.4 mV) at 14.57 nW and 69.7 ps ($1 \to T$ t_{pd} = 1,540.6 ps, matched $T \to 1$ t_{pd} = 628.0 ps vs. 527.0 ps baseline). In EXP-05C, triple-well 28T q27_STI_HF_TW (196 R/197 C, verified dnwell pwell=V_{MID}) passes 75/75 PEX DC-window corners ($\geq$ 15.43% V_{DD}, 14.6 nW, matched 0.65–1.15 V 54.6 ps) and reduces worst of six PEX arcs at sf/−40°C/1.62 V by 3.08× (18.89 $\to$ 6.13 ns; schematic max 4.29 ns occurs at ss cold). In nominal externally kicked transients of 5 composed extracted stages, baseline 20T q27_STI

TABLE I
EXP-05/05B–05L Extracted SKY130A Cells (9 Baseline + 16 Q27-Compiled = 25/25: 0 DRC, Unique LVS; *nwell=V_{MID}; †dnwell Netgen LVS)

SKY130A Cell	Tx	Area [μm^2]	Magic RC	ΣC [fF]
q27_NTI	2T	66.8	9R/13C	6.3
q27_PTI	2T	66.8	9R/13C	8.0
q27_BINV	2T	66.8	9R/13C	6.7
q27_NAND2	4T	66.8	19R/28C	8.0
q27_TGATE	2T	66.8	8R/22C	8.2
q27_TGATE_WEAK	2T	66.8	8R/22C	7.9
q27_TGATE_ACC	2T	66.8	4R/27C	8.0
q27_TMUX	20T	601.4	117R/136C	95.2
q27_STI	20T	601.4	119R/116C	93.8
q27_STI_HF*	29T	1033.1	202R/189C	172.0
q27_STI_HF_TW†	28T	1016.0	196R/197C	185.5
q27_TSRAM_46T	46T	1477.8	298R/312C	294.3
q27_TSRAM_56T_HF*	56T	2024.9	398R/403C	380.1
q27_TSRAM_60T_Z3*	60T	2596.7	436R/431C	483.0
q27_KLEENE_GUARD_60T	60T	1813.8	348R/366C	336.6
q27_KLEENE_GUARD_HF*	42T	1405.7	288R/285C	247.1
q27_TMUL_Z3*	68T	2582.1	434R/469C	490.3
q27_THA_Z3*	100T	3190.0	589R/691C	606.6
Periphery total (7 cells)	60T	2288.3	418R/465C	351.8

quenches to 0.900 V, whereas q27_STI_HF (81.2 MHz), q27_STI_HF_TW (85.9 MHz), and 3-state CYCLE_UP (192.2 → 77.5 MHz, 2.48× PEX) sustain rail-to-rail oscillation.

V. Decoupled T-SRAM, 2D Array, SEU, and Kleene Guards

Shared-port T-SRAMs (44T SKY130A and 6T BTBT [6]) suffer read-disturb collapse (Read-SNM$_0$ = 0.0 mV) under V_{DD}-precharged bitlines (Fig. 5a). A 2T decoupled read port (46T SKY130A; 8T BTBT) restored modeled Read-SNM$_0$ to 350.1 mV in SKY130A (350.06 mV from composed extracted leaf cells) and 368.0 mV in the BTBT model, while keeping small transient disturbs nonzero. Extracted q27_TSRAM_46T (EXP-05D, 0.001 mV disturb) draws 29.1 μW in state 0. Weak-driver sub-rail keepers (q27_TSRAM_56T_HF, EXP-05E, 0.01 mV disturb) lower state-0 standby 999× to 29.1 nW, though rail states draw ≈ 10.9 μW. Replacing ratioed shifters with dual sub-rail 4T DCVS shifters (q27_TSRAM_60T_Z3, EXP-05I/J) reduces all-three-state TT standby to 12.95/13.55/12.94 nW (804× worst-state reduction, 5/5 PVT, 0.363 mV max disturb). In 72-finger Pelgrom mismatch runs (EXP-05J), 60T_Z3 passed 500/500 TT ($p_{99} \leq 17.15$ nW) and 498/500 (99.6%) sf/−40°C samples (2,996/3,000 state trials). In a 2×2 (224T, 4×56T) PEX array (EXP-05F), column half-select disturb is 7.12 mV (114.63 nW four-cell state-0 standby); floating V_{MID}-precharged row half-select retained at the sampled 300 fF point and failed at 500 fF (2D wordline gating: 0.37 mV at 200 fF). Cold-start SC 2:1 co-simulation (100 MHz / 120 ns boot, 5 corners, ≤ 23.81 mV ripple) with a 0.85× replica pfet_lvt load lifts adjacent RBL-level separation 2.91× (165.3 → 481.25 mV, ≤ 0.375 mV disturb). In EXP-05G, 7 Q27-compiled periphery/StrongARM macros with dummy-bitcell midpoint tracking lift worst 5-corner comparator differential overdrive 3.86× (62.8 → 242.5 mV), restoring DOUT in 0.57–1.36 ns (422.6 fJ/trit TT) and passing 3,000/3,000 Pelgrom mismatch state trials across modeled ss/125°C and sf/−40°C corners ($A_{VT} = 5$ mV·μm).

Double-exponential current injections [17] ($\tau_r = 20$ ps, $\tau_f = 200$ ps, $C_{node} = 5$ fF, storage-node flip criterion after physical Write→Hold without uic, Fig. 5b) quantify state-0 SEU asymmetry: 44T SKY130A gives $Q_{crit}(0^+) = 33.20$ fC vs. $Q_{crit}(T) = 74.78$ fC (2.25×), while a 1.8 V/50 nA BTBT model (distinct from Table V's 1.0 V/18 nA profile) gives 4.256 vs. 93.331 fC (21.9×). For 60T_Z3 PEX (EXP-05J, integrating verification pulses at 1.03× the bisection upper amplitude), state-0 Q_{crit} is 125.5–131.5 fC at $\tau_f = 200$ ps while rail states survive the tested > 2.2 pC bound at 200 ps; at $\tau_f = 1$ ns, recorded upsets occur at 743.9 fC ($T \to 0$), 793.4 fC ($0 \to T$), and 1,906.3 fC ($+1 \to 0$). Across six directed single-lane disagreements, q27_KLEENE_GUARD_60T (Fig. 5c) settles to safe 0 in ≤ 0.272 ns schematic / ≤ 0.626 ns PEX with zero $-1 \leftrightarrow +1$ inversions; 42T q27_KLEENE_GUARD_HF (EXP-05H, −22.5% area) settles in ≤ 1.31 ns TT PEX while reducing TT state-0 standby 1,658× (43.6 μW → 26.3 nW).

VI. Q27 v3.2.28 Compiler, TDD+TMG, and Track-B ML

A. Q27 v3.2.28 SSOT Compiler & Native Core Integration

Q27 v3.2.28 compiles typed physical descriptions (circuit/well/mos/inst/soc) and pipelined Track-B datapaths (datapath) into bit-identical (compile-twice SHA-256) SPICE, GDSII, LEF 5.8/Liberty .lib (20 exported macro types currently; 17 in initial EXP-09C), and Verilog-2001. Nine parse-time guards (Table II) caught 17/17 seeded errors.

Table III summarizes four progressively scaled native OpenROAD/KLayout floorplans (EXP-09C/D–09G), each passing 0 PDN/route/antenna/sky130A_mr.drc violations and top-level Magic 8.3/Netgen LVS UNIQUE MATCH. In EXP-09C, the reported 114.0 nW leakage and +6.028 ns slack come from Liberty macro abstracts with fitted timing tables (not independent full-chip ternary timing validation), and 09D's 2.01 mV figure is a monitored internal rail deviation rather than a chip-wide IR bound. In EXP-09G (834 fingers, 8,711 R/6,981 C, 13.045 pF), a 707T compute-near-memory core produced four directed two-term dot products ($3c_{out}+s = A_0W_0 + A_1W_1 \in \{-2, +2, 0, +1\}$; −1 untested) across 3/3 runs (TT, ss/125°C, and TT-with-SC) using external sensing references, bitline precharge/load devices on exposed internal nodes, clocks, and off-core SC 2:1 components (2×36 pF flying, 32 pF tank); no stateful accumulation or network inference was exercised. Preset testbench activation-ramp-end to output-sample intervals for cascaded TMUL→THA phases B/C are 24.8/20.3 ns (TT) and 46.8/24.3 ns (SS-hot) (not threshold-extracted settling delays), with 21.8 ns post-SAE in phase A and 42/55 ns post-read before standby sampling; SS-hot mixed/all-zero standby reached 2.09/3.10 μW, while the 09G SC run

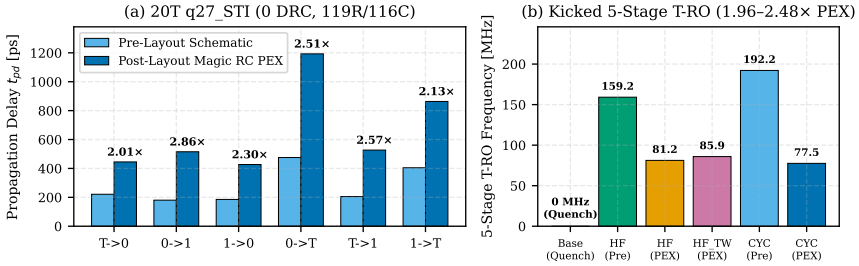

Fig. 4. EXP-05/05B/05C Pre vs. Magic 8.3 RC PEX: (a) 20T q27_STI 6-arc delay scaling (2.01–2.86×); (b) Nominal externally kicked 5-stage composed T-RO frequencies showing baseline quench vs. sustained PEX oscillation in q27_STI_HF (81.2 MHz), q27_STI_HF_TW (85.9 MHz), and CYCLE_UP (77.5 MHz).

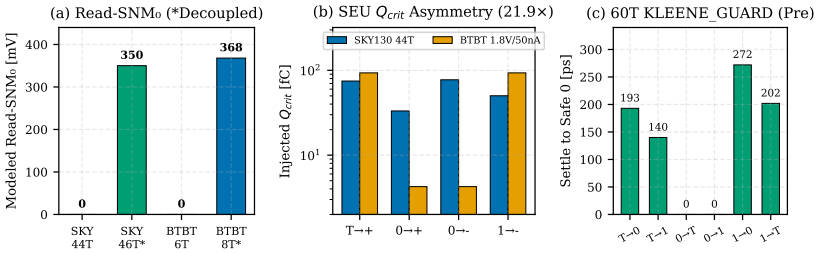

Fig. 5. EXP-07 T-SRAM & fault injection: (a) 2T decoupled port restores modeled Read-SNM$_0$ ($0 \rightarrow 350.1/368.0$ mV); (b) Injected double-exponential Q_{crit} asymmetry in 44T SKY130A (2.25×) and 1.8 V/50 nA BTBT (21.9×); (c) Schematic 60T KLEENE_GUARD settling across 6 directed single-lane disagreements (≤ 0.272 ns pre, ≤ 0.626 ns PEX).

TABLE II
Q27 v3.2.28 Compile-Time Checks (17 Seeded Errors Detected)

Guard	Physical / Structural Invariant Enforced	Det.
Q27-E101	nwell.2a$\geq$ 1.27 μm & dnwell.1$\geq$ 3.0 μm	3/3
Q27-E102	SI dimension check, 5 nm grid, SKY130 min W/L	3/3
Q27-E103	Direct rail shorts ($V_{DD} \leftrightarrow V_{SS}$) & floating gates	2/2
Q27-E104	Hierarchical inst port-arity & cyclic recursion	2/2
Q27-E105	pack5 alignment, overflow proof, SI clock/stages	3/3
Q27-E106..109	SoC overlap/keepout, V_{MID} PDN, via4/m5, nets	4/4

TABLE III
Native OpenROAD/KLayout Core Integrations (TT Ideal-V_{MID} Standby; Separate Cold-Boot SC 2:1 Ripple; 0 DRC, Unique LVS)

Exp. (Core)	Inst/Tx	Footpr. [μm]	Mix/0 [nW]	SC [mV]
09C/D (orig.)[a]	11/215	280×156	—/440.94	3.82
09E (2×2 bank)[b]	23/471	464×184	420.25/242.10	16.78
09F (2 lanes)[c]	25/607	464×216	422.73/241.10	9.576
09G (dot core)[d]	26/707	464×250	250.15/244.52	17.238

SC clock/boot: [a]100 MHz/110 ns; [b]100/45; [c]50/60; [d]33.3 MHz (30 ns)/60 ns.

averaged 272.94/516.41 nW over a 5 ns sample window of a 30 ns SC period on sensed supplies that also power external bitline precharge/load devices (whereas 09D's converter-inclusive draw was 70.2 μW over 3 ns of a 10 ns cycle; full regulated standby requires whole-cycle converter and clock energy).

For Track-B RTL, Q27 enforces the 2-bit ABI (2'b11=T, 2'b00=0, 2'b01=+1, 2'b10=invalid) and radix-243 pack5 packing. Using Yosys 0.62's MiniSat solver (sat -verify -prove, 14,956 vars / 39,428 clauses, 0.18 s), we proved that pack5_unpacker_safe asserts fault_invalid_pack5=1 and clamps outputs to 0 for bytes 243–255 with no 2'b10 outputs across bytes 0–242 (this miter verifies decoder fault/clamp and legal encodings, not valid-byte arithmetic equivalence or pipelined MAC datapaths).

B. Native TDD+TMG Synthesis, Track-B ML, and SKY130A P&R

Q27 combines Reduced Ternary Decision Diagrams (TDDs), Rudell dynamic variable sifting [18], and Ternary Multi-valued Gate (TMG) mapping (STI/PTI/NTI/CYCLE/TMIN/TMAX), checking every TDD against its truth table in $\{-1, 0, +1\}^n$. On a 5-input selector (T_SIFT5, 243/243 vectors), sifting reduces TDD nodes from 36 to 7 (−80.6%), and TMG mapping reduces to 5 gates (−86.1% combined). Across 10 ternary circuits in Yosys 0.62 (sky130_fd_sc_hd, Fig. 6a), estimated 28-nm BTBT transistor counts are 1.15–6.5× lower than estimated binary Yosys counts (T_FA: 100 vs. 160 tx, 30.0 vs. 153.9 μm^2; NTRU_GF3_MAC: 36 vs. 125 tx, 10.8 vs. 117.6 μm^2). A 27-trit vs. 43-bit adder uses 36.6% fewer I/O signals (83 vs. 131) and exposes a 3.05× binary-emulation area ratio (4,188 vs. 1,373 μm^2).

In EXP-09 (Table IV, Fig. 6b), Yosys 0.62 synthesizes two unpackers and five 10-weight × 8-bit activation MACs (sky130_fd_sc_hd and xc7 -nodsp, summing LUT1–6 as xc7 LUTs). Unchecked combinational tmac_10w_pack5 (6,261 μm^2, 451 xc7 LUTs, 0 DSP48) saves 58.3% ASIC area, 57.5% xc7 LUTs, and 60.0% fewer encoded weight bits vs. INT4 (15,013 μm^2, 1,060 LUTs); tmac_10w_pack5_safe (6,429 μm^2) adds +2.68%

TABLE IV
EXP-09 Yosys 0.62 ASIC (sky130hd) & FPGA (xc7 -nodsp, LUT1–6 Sum)

Unpacker / 10W MAC	Cells	Area [μm^2]	xc7 LUTs	CARRY4
pack5_unpacker	161	958.4	36	0
pack5_unpacker_safe	167	943.4	39	0
tmac_10w_pack5	918	6261.0	451	34
tmac_10w_pack5_safe	966	6428.7	471	34
tmac_10w_2bit	650	4379.2	490	44
mac_10w_int2	435	6730.2	443	4
mac_10w_int4	828	15013.1	1060	4

ASIC area (−57.2% vs. INT4). Against unpacked 2-bit ternary (tmac_10w_2bit: 4,379 μm^2, 490 LUTs), pack5 trades +43.0% combinational ASIC area for −8.0% xc7 LUTs and −20.0% encoded weight bits (1.60 vs. 2.00 b/w); relative to Signed_INT2 (6,730 μm^2), pack5 uses −7.0% ASIC area, −20% weight bits, and +1.8% LUTs (451 vs. 443). On one synthetic 512×512 Gaussian matrix with floating-point activations (30.98% observed zeros; $p_0 = 55\%$ used elsewhere is an assumption), absmean ternarization gave 5.82 dB SQNR (identical for packed and unpacked weights) vs. 2.07 dB for the tested per-tensor INT2 quantizer (+3.75 dB, attributable to the quantizer rather than pack5). Finally, EXP-09B routed the 2-stage q27_TMAC_10W_PACK5_SAFE_PIPE through LibreLane 3.0 (19,130.8 μm^2 stdcells, 2,257 cells, 47,129.7 μm^2 floorplan). At a 12 ns (83.33 MHz) target across 9 OpenSTA corners, the routed block passed setup (worst slack +2.701 ns, WNS = 0), hold (+0.175 ns, WNS = 0), and electrical checks (0 max-slew, 0 max-capacitance, 0 max-fanout via multi-corner CTS/resizer repair excluding SKY130HD delay lines and 1× buffers). Separately, layout verification passed Magic/KLayout/route DRC, Netgen LVS, and antenna checks with 0 violations. Slack-derived frequency estimates are 107.5 MHz (ss/100°C/1.60 V) and 214.8 MHz (tt); at 83.33 MHz and 3.904 mW default-activity TT STA power, estimated efficiency is 0.427 TOPS/W under 20 MAC-equivalent ops/cycle (or 0.406 TOPS/W under literal RTL counting of 10 signed products + 9 additions = 19 ops/cycle).

VII. EXP-10: Cross-Technology PPA Map & Related Work

Combining matched isolated-supply SKY130A PEX metrics, EXP-04 SC 2:1 ratios, assumed Track-B standard-cell gate reference constants (0.45 nW, 18.2 fJ, 145 ps, distinct from routed-block EXP-09B STA), and analytical/literature projections (22FDX back-gate scaling, assumed 28-nm BTBT profile with $V_{DD} = 1.0$ V, $P_{\text{stat}}(0) = 18$ nW, $E_{\text{sw}} = 3.6$ fJ, and $t_{pd} = 85$ ps informed by 28-nm BTBT capacitance modeling [7], and 7-nm CNTFET [9]), Table V and Fig. 7 evaluate per-gate power at $f_{\text{clk}} = 100$ MHz via $P_{\text{gate}}(p_0) = [E_{\text{sw}} f_{\text{clk}} \alpha_{\text{gate}} + P_{\text{stat}}(0) p_0](1 + \eta_{\text{reg}})$ with $\alpha_{\text{gate}} = 0.25(1 - p_0)$ (state-0 static + dynamic only; nonzero-state leakage omitted) and the analytical bus energy model

$$E_{\text{bus}}(L) = \Big[N_w C_w L V_{DD}^2 \alpha_{\text{eff}} + N_w E_{\text{drv}}\Big](1 + \eta_{\text{reg}}) \quad (1)$$

with $N_w = 43$ binary vs. 27 ternary payload wires (−37.2% payload wires vs. 36.9% asymptotic bound; physical layouts also allocate shield/supply tracks), $\alpha_{\text{eff}} = 0.25$ (binary) vs. $0.25(1 - 0.5p_0)$ at assumed $p_0 = 0.55$, and a +25% 0-shield capacitance factor applied to ternary wires at both 130 nm ($C_w = 140$ vs. 175 fF/mm @ 1.8 V, $E_{\text{drv}} = 18.2$ vs. 98.5 fJ, $\eta_{\text{reg}} = 1.25\%$) and 28 nm ($C_w = 180$ vs. 225 fF/mm @ 1.0 V, $E_{\text{drv}} = 2.4$ vs. 3.6 fJ, $\eta_{\text{reg}} = 0\%$):

- Power vs. p_0 (Fig. 7a): Using isolated single-DUT matched 6-arc mean PEX switching energies (static-subtracted in both producers: 136.36 fJ baseline 20T vs. 309.10 fJ q27_STI_HF; same-arc $T \to 1$: 120.69 vs. 265.26 fJ), at $p_0 = 0.55$ q27_STI_HF (3.53 μW/gate) avoids the 20T baseline's 14.573 μW state-0 static draw (9.67 μW/gate at $p_0 = 0.55$, 2.74× higher) and decreases with p_0, while remaining 17.2× above the assumed 130-nm Track-B reference gate model (0.205 μW/gate); projected 28-nm BTBT (0.050 μW) and 22FDX (0.057 μW) reach ≈ 0.05 μW/gate.
- Global Bus Crossover (Fig. 7b): Under (1), 130-nm 27-trit 0-shielded buses intersect 43-bit binary at $L \approx 0.924$ mm (0.902–0.963 mm over 0.37–2.74% positive SC 2:1 overhead). Under the assumed 28-nm driver energies, ternary is lower already at $L = 0$ (97.2 vs. 103.2 fJ) with a shallower slope, so no crossover occurs for $L \geq 0$.

Table VI compares representative 2019–2026 ternary works by implementation, evidence level, and demonstrated function. Fabricated silicon demos include BTBT devices [5], P-TMOS [8], 40-nm charge-domain ternary CNN [12], and 28-nm ternary-latch CIM [13]; circuit/library works span T-CMOS full adders/sequential logic [6], compact BTBT memory [7], CNTFET/CMOS MVL arithmetic [10], [11], FPGA inference [2], and CPU/GPU edge kernels [3]. Q27-Trilith's distinct scope is an end-to-end compiler-to-extracted-layout SKY130A demonstration paired with Track-B pack5 synthesis and P&R.

VIII. Limitations, Access, and Threats to Validity

Four boundaries govern these results: (1) No Q27 die was fabricated. Across EXP-01..10, only the 25 cells in Table I (9 Python-constructed baselines + 16 Q27-compiled) and four cores in Table III underwent SKY130A RC PEX; other studies (EXP-01..04, 06B, 07) use schematic/behavioral models or composed extracted stages. In planar 130-nm SKY130A, an estimated 27-trit native multi-V_{th} adder occupies 15,536 μm^2 (26,690 μm^2 scaled to q27_STI_HF) vs. 1,373 μm^2 for a 43-bit binary sky130_fd_sc_hd adder (11.3–19.4×), motivating Track-B pack5 for near-term binary silicon and 22FDX/28-nm BTBT for native density. (2) 22FDX, 28-nm BTBT, and 7-nm CNTFET figures are analytical/literature projections [7], [9]; EXP-02/07's empirical 1.8 V/50 nA BTBT deck differs from Table V's 1.0 V/18 nA profile. (3) Planar q27_STI_HF incurs 18.89 ns worst PEX arc delay at

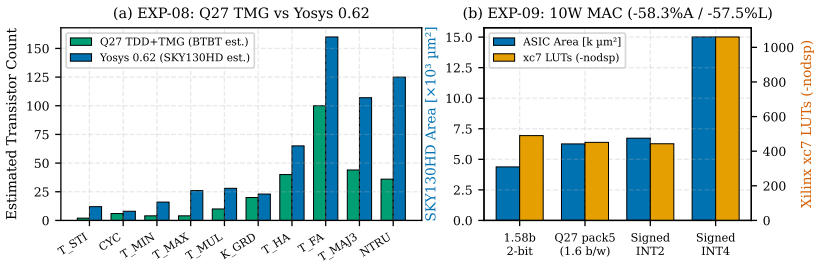

Fig. 6. EXP-08/09 Yosys 0.62 benchmarks: (a) Estimated native Q27 TDD+TMG (BTBT) vs. binary sky130_fd_sc_hd counts across 10 circuits; (b) Track-B combinational tmac_10w_pack5 saves 58.3% ASIC area and 57.5% xc7 LUTs (-nodsp) vs. INT4.

TABLE V
EXP-10 Cross-Technology PPA Summary (Matched Isolated SKY130A 6-Arc Mean E_{sw} & $T \to 1$ PEX Delay; Projections Tagged [Model])

Technology Track	Node [nm]	V_{DD} [V]	STI / T-SRAM	$P_{stat}(0)$ [nW]	E_{sw} [fJ]	t_{pd} [ps]	Qualification / Scope
SKY130A 20T STI Baseline (PEX)	130	1.80	20T/46T	14573.0	136.36	527.0	55/75 pre DC (≥15%)
SKY130A 29T q27_STI_HF (PEX, Ours)	130	1.80	29T/60T	14.57	309.10	628.0	75/75 PEX DC + 1k pre MC
22nm FD-SOI Back-Gate [Model]	22	0.90	10T/18T	3.2	4.80	42.0	Projected (back-gate ABB)
28nm T-CMOS BTBT [Model]	28	1.00	2T/8T	18.0	3.60	85.0	Projected (compact model)
7nm-eq CNTFET / FeFET [Model]	7	0.75	6T/10T	8.5	0.65	24.0	Projected (literature)
Track B: SKY130HD pack5*	130	1.80	12T/10T	0.45	18.20	145.0	Block STA: 0/0/0 (9c)

*Track-B per-gate $P_{stat}/E_{sw}/t_{pd}$ (0.45 nW, 18.2 fJ, 145 ps) are assumed standard-cell reference constants, distinct from the routed EXP-09B block STA.

TABLE VI
Comparison With Selected Ternary Device, Circuit, and Accelerator Works (2019–2026)

Work / Venue	Implementation	Evidence	Demonstrated Function
Jeong et al., Nat. Electron. '19 [5]	Wafer BTBT T-CMOS	Measured silicon	Ternary inverter and latch
Ko et al., TCAS-I '23 [6]	T-CMOS (compact model)	SPICE simulation	42T full adder, sequential circuits, 6T T-SRAM
Choi et al., JEDS '25 [7]	28 nm BTBT compact	Meas. + SPICE model	Compact capacitance model for on-chip memory
Han et al., EDL '25 [8]	TS-integrated P-TMOS	Measured device	Tunable mid-state ternary inverter
Zhao/Wen et al., TETC'24/TCSI'25 [10], [11]	CNTFET / CMOS MVL	Schematic SPICE	Ternary arithmetic and approximate MAC
Yang et al., JSSC '23 [12]	40 nm charge-domain	Measured silicon	In-memory charge-domain ternary CNN chip
Kim et al., A-SSCC '24 [13]	28 nm ternary-latch CIM	Measured silicon	Sparsity-aware CIM, 323 TOPS/mm^2/b, 2007 TOPS/W/b
TerEffic '25 [2]	FPGA accelerator	FPGA hardware	Binary-hosted ternary LLM inference accelerator
TABv2, TVLSI '26 [3]	CPU/GPU SW library	Edge SW bench	Faster ternary/binary neural inference kernels
Q27-Trilith (v3.2.28, Ours)	SKY130A 3-rail + Track-B	Open-PDK PEX/P&R	Compiler, 25 PEX cells, 707T dot core, pack5*

*75/75 PEX inverter DC PVT, 1k pre MC, externally supported 707T dot core; Track-B pack5 passes 9-corner OpenSTA (0/0/0 slew/cap/fo) and physical DRC/LVS/antenna.

sf/−40°C/1.62 V due to $V_{sb} = V_{MID}$ body effect; triple-well q27_STI_HF_TW lowers this to 6.13 ns (3.08×) at the cost of dnwell guard-ring area. Single-layer EXP-09 SQNR evaluates projection quantization fidelity rather than full-model perplexity [1], [2]. (4) Replaying archived JSON reports requires only the verification scripts, whereas re-running simulations requires pinned SKY130A (open_pdks 1.0.620) and LibreLane 3.0.14 Docker digests (documented in ARTIFACT_EVALUATION.md, including the container sky130A.tech version patch and optional external EXP-01 33T deck). Full Q27 v3.2.28 (v3.2.28-cycle71) source and GDSII artifacts are archived under restricted access to preserve priority rights, with reviewer access available upon request.

IX. Conclusion

Q27-Trilith (v3.2.28) demonstrates an end-to-end compiler-to-extracted-layout flow across 25 DRC-clean, LVS-matched SKY130A ternary cell types (9 baseline, 16 Q27-compiled; 2T–100T), anchored by a sub-rail 29T inverter reducing nominal tt matched both-supply PEX state-0 static power ≈ 1,000× to 14.57 nW while passing 75/75 extracted DC-window PVT corners (≥ 15.43% V_{DD}). At the macro level, a 707T compute-near-memory core verified four directed two-term dot products $(-2, +2, 0, +1)$ at 250.15/244.52 nW TT mixed/all-zero standby (2.09/3.10 µW SS-hot) with external sensing and mid-rail support under preset testbench sampling windows (24.8/20.3 ns TT and 46.8/24.3 ns SS-hot for cascaded phases B/C). On Track B, Q27-compiled pack5 cuts 10-weight MAC synthesis area by 58.3% and xc7 LUTs by 57.5% vs. INT4 (+43.0% area / −8.0% LUTs / −20% weight bits vs. unpacked 2-bit ternary), and closes LibreLane 3.0 SKY130A P&R with 0/0/0 max-slew/cap/fanout and 0/0 setup/hold WNS across 9 Open-

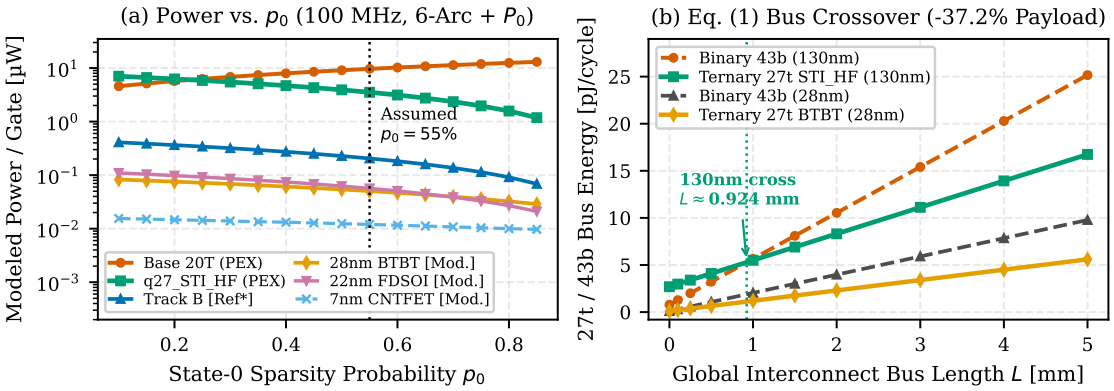

Fig. 7. EXP-10 cross-technology PPA map: (a) Modeled per-gate power vs. p_0 at 100 MHz using matched isolated 6-arc mean SKY130A PEX energies (state-0 static + dynamic; nonzero-state leakage omitted); (b) Eq. (1) bus energy crossover ($L \approx 0.924$ mm at 130 nm; 28-nm BTBT lower for all $L \geq 0$ under assumed driver energies).

STA corners plus 0 physical DRC, LVS, and antenna violations (107.5/214.8 MHz SS/TT, 0.427 TOPS/W at 20 MAC-eq ops or 0.406 TOPS/W at 19 literal ops).

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